FIG. 29

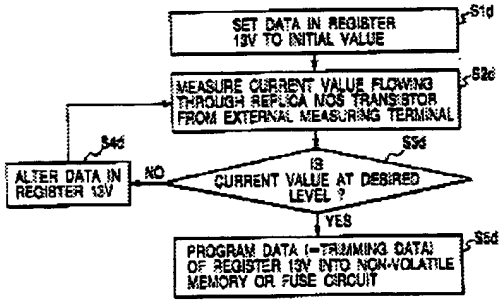


FIG. 30(A)

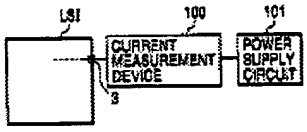
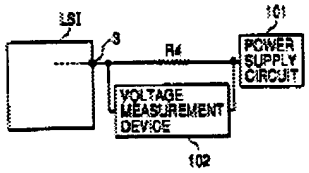


FIG. 30(B)



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high ... s thereof, with a
long... me achieved
in t... uctor storage.

TITLE - 11 (1):

Semiconductor memory device with capacitor over non-volatile memory cell gate structure

Brief Summary Text - BSTX (3):

The present invention relates to a semiconductor memory device which combines a volatile semiconductor storage with a nonvolatile semiconductor storage.

Brief Summary Text - BSTX (5):

A conventional semiconductor memory device of the type referred to above is constructed in such a manner as shown in, for example, FIG. 3. Specifically, the semiconductor memory device of FIG. 3 has a nonvolatile semiconductor storage, a control unit and a volatile semiconductor storage formed on a P-type semiconductor substrate 21. The nonvolatile semiconductor storage is provided with a transistor M2 comprised of a drain area located at one end of an n-type impurity diffusion layer 22, a floating gate

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Fig. 2

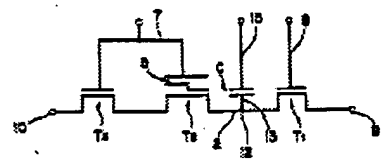
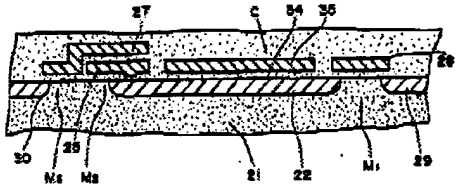


Fig. 3 (PRIOR ART)



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regi... OM memory cell
arra... generating
mean... supplying means of
the ... age system
of t... y are formed and to
whic... op is
applied is surrounded by a p-well region as small as possible. This structure avoids latch up caused by a floating substrate.

Brief Summary Text - BSTX (56):

In a semiconductor integrated circuit for a microcomputer according to the third invention, a supply voltage Vcc system which includes a CPU, a ROM, a RAH, an input/output unit, and EEPROM control systems and to which a high voltage Vpp is not applied is formed in a twin-well region. This structure realizes a line width of 1 .mu.m or less, enables micromachining of a circuit, and improves the degree of integration. On the other hand, a portion which includes an EEPROM memory cell array and an EEPROM peripheral high-voltage system and to which the high voltage Vpp is applied is formed, for example, on a p-type semiconductor substrate and has an NMOS structure. This structure minimizes a substrate effect, and enables a charge pump, Vpp switches, and memory cells to operate normally.

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FIG. 10A
PRIOR ART

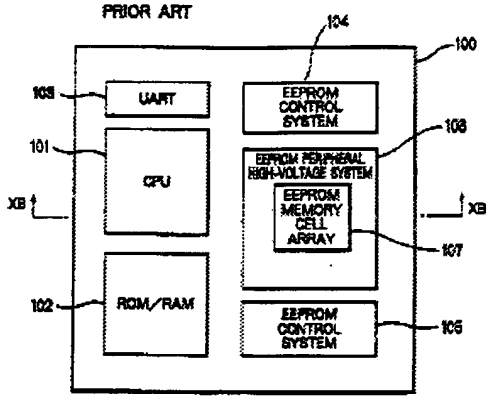
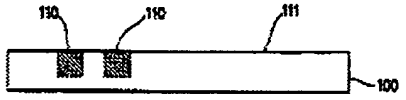


FIG. 10B
PRIOR ART



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